



## TECHNICAL DATA

|  |  |
|--|--|
| Type of receiver/radar                                   | coherent on receive with MTI   |
| Frequency range  | 150-170 MHz  |
| Intermediate frequency                                   | 10.7 MHz   |
| optionally   | 21.4 MHz   |
| Noise figure   | 2.8  |
| Dynamic range  | 80 dB  |
| Sensitivity  | -113.5 dBm for:<br>Pd=0,9 (probability detection)<br>Pfa =10 <sup>-6</sup> (false alarm probability) |
| COHO   | digital, based on phase prediction<br>in processing algorithm  |
| Sampling rate (variable)                                 | 32.1 to 80 MSamples/s<br>with resolution of 14 bits  |
| Sampling rate at the digital<br>IF block output          | 0.8 MSamples/s   |
| IAGC   | controllable   |
| Number of DSP processors<br>in digital LF block          | 5<br>or using IRITEL FPGA platform   |
| RF protection of receiver                                | limiter with protector   |
| Intentional and unintentional<br>interference protection | by software<br>reconfiguration   |
| Output signals   | linear (LIN) video signal<br>logarithmic (LOG) video signal<br>video trigger pulse                   |

|   |   |               |
|---|---|---------------|
| Output signal levels (connection with<br>extractor and video indicator) | video signals   | -0.7 V to 6 V |
|   | trigger   | 0 to 5 V      |
| Selection of digital<br>clutter cancellation type                       | realized by software<br>reconfiguration with<br>option to turn off MTI function |               |

### SOFTRAD

#### *IRITEL FPGA evaluation and development platform upgrade of VHF DR/P-12/18*

- PCI 2.2 compatible
- FF1152 Xilinx Virtex-II FPGA, up to eight-million gates
- 2 x 105 MSPS 14-bit A/D converters
- 2 x 150 MSPS 14-bit D/A converters
- Programmable clock solution
- Two expansion 80-pins ports, TI daughter card expansion specification compatible
- DIMM 184 DDR SDRAM slot (up to 1 GB)

SOFTRAD platform



Analog block of receiver



# VHF DR/P-12/18 DIGITAL RADAR RECEIVER

- Reception and processing of radar signals in 150-170 MHz range
- Software reconfiguration of the receiver based on the software radar concept
- Remote control applications
- Universal solution for P-family of radars P12/P14/P15/P18
- IRITEL FPGA platforms upgrades of VHF DR/P-12/18 (SOFTRAD/Virtex II and Spartan 3)
- Keystone for P-family of radars modernization



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## Application

VHF DR/P-12/18 is the digital radar receiver developed for the replacement of existing P-12/18 radar receivers with software defined receiver which has better performances. It is intended for reception and processing of radar signals in 150-170 MHz range.

VHF DR/P-12/18 can be easily adapted for other types of radars by modification of only analog RF block.

Optionally, remote control applications are included:

- Remote control of digital radar receiver VHF DR/P-12/18
- Signals forwarding from receiver VHF DR/P-12/18 to digital indicator on separate location

Remote control of P-12/18 radar shelter (with mounted VHF DR/P-12/18) is realized via the optical cable at distances from 100 to 500 m by using optical line terminals - optical transmitter and receiver of IRITEL production program.

The receiver supports multi static operating mode.

## Configuration

Digital radar receiver VHF DR/P-12/18 contains:

- Analog RF/IF block mounted in rack (width 19" and height 2H) with intelligent front panel (keyboard and display)
- Digital IF/LF block mounted in rugged central computer, type PC ADVANTECH (also in 19" shock-absorbed rack)

## Analog block of receiver

- RF limiter for receiver protection from high level input RF signals during emissions

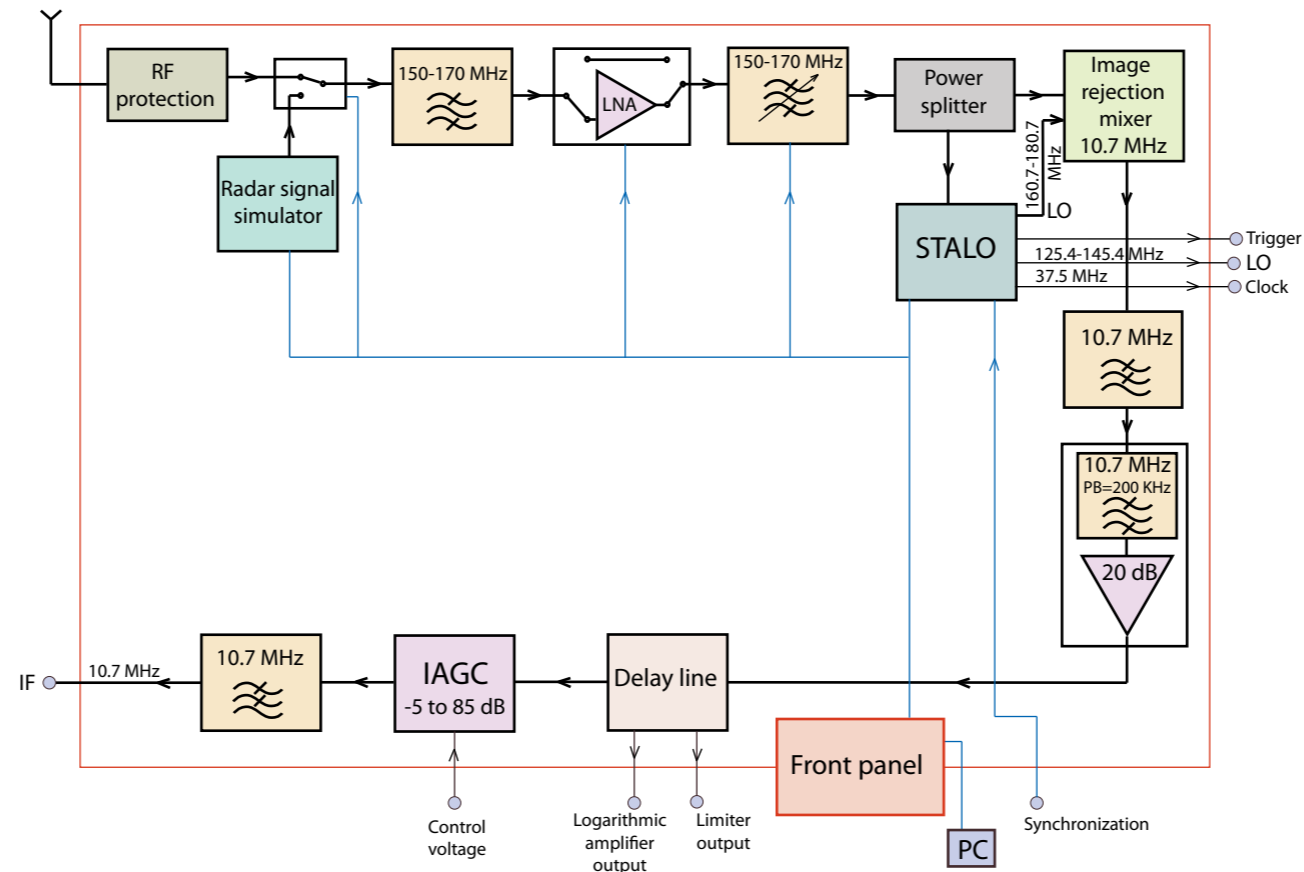
- RF passband filter for 150-170 MHz



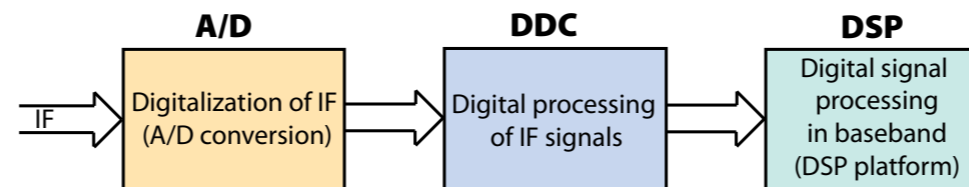
- Low-noise RF amplifier



## Analog block of receiver



## Digital block of receiver



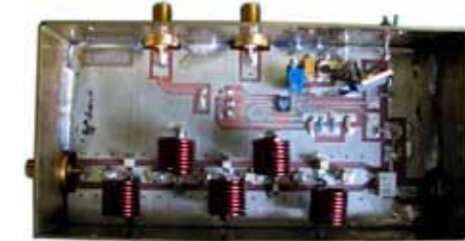
- Adjustable RF filter RFVAR
- Local oscillator with automatic adjustment to the transmitted signal frequency (STALO)
- Image Rejection Mixer
- IF passband filter at 10.7 MHz



- IAGC amplifier



- Delay line



- Radar signal simulator for receiver testing

## Digital block of receiver

### A/D Module

- A/D conversion of IF signal

### DDC Module

- Extraction of I, Q signal components
- Decimation
  - decrease of sampling rate
  - filtering

### DSP Module

- Calculation of radar echoes phase based on the memorized transmitted pulse phase
- Calculation of radar echoes amplitude based on the AGC setting
- Echoes matrix creation of N transmitted pulses
- MTI filter (clutter cancellation)
- CFAR algorithm